Remarks

Claims 1-21 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The instant Office Action indicated the following rejections: claims 1-7, 11, 13-16 and 19-21 stand rejected under 35 U.S.C. § 103(a) over Mitsuhira *et al.*(U.S. Patent No. 5,155,853) in view of standard register use, as evidenced by Yoshida (U.S. Patent 5,450,566); claims 8-10 and 17-18 stand rejected under U.S.C. §103(a) over Mitsuhira and standard register use, as applied supra, in view of Fujimura (U.S. Patent No. 5,751,988); and claim 12 stands rejected under U.S.C. § 103(a) over Mitsuhira and standard register use, as applied supra, in view of standard debugging techniques, as evidenced by Hohl *et al.*(U. S. Patent No. 6,035,422).

With regards to the 35 U.S.C. § 103(a) rejections of claims 1-21, Applicant respectfully submits that the Examiner has not presented a *prima facie* case of obviousness. To establish a prima facie case of obviousness the prior art reference (or references when combined) must teach or suggest all the claim limitations. To begin with, Applicant notes that the Examiner's response does not show correspondence to (nor even mention) each claim limitation. Instead, the argument is merely a recitation of a few elements without further explanation of those claim limitations which are not addressed. M.P.E.P. 2141.02 states that "the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." M.P.E.P. 2141.02 further states that "(d)istilling an invention down to the 'gist' or 'thrust' of an invention disregards the requirement of analyzing the subject matter 'as a whole.'" Applicant submits that merely showing that register data is used in arithmetic operations fails to address each claimed limitation.

For example, the Examiner's response fails to address limitations directed to specific uses of special function registers. Applicant previously presented the failings of the Mitsuhira reference with regards to such limitations in the response of September 7, 2007, which is fully incorporated herein by reference. A proper analysis of the claim limitations (see Applicant's argument of September 7, 2007) is not rendered moot simply because data from a register is at some point used in an arithmetic operation. For instance, the Examiner's response fails to mention special function registers and a word

search of the newly asserted Yoshida reference reveals that special function registers are not mentioned. Accordingly, the Final Office Action is non-responsive and fails to present a *prima facie* case of obviousness. Applicant respectfully requests that the rejections be removed.

Moreover, the Examiner argues that it would have been obvious to combine register contents with arithmetic operations of Mitsuhira because use of registers allows for enhancements, such as efficient use of register addressing modes. Applicant is unable to ascertain what the Examiner's alleged modification of Mitsuhira involves. As such, Applicant can not be certain what the Examiner has intended the combination to include. Applicant requests clarification as to what is being modified in the Mitsuhira reference, to the relevance of such a vague combination of registers and arithmetic operations in view of the claim limitations, and to how such an advantage would be seen in the modified Mitsuhira reference. For instance, to the extent that register data is being used in arithmetic operations the Examiner has not provided information explaining and the references are unclear as to: what registers are being referenced; where the arithmetic operations are to be implemented, and how efficient use of register addressing modes would be seen as a result of the combination. Applicant respectfully submits that the Examiner's combination is merely recitation of various elements without a proper analysis of how the elements would be combined. Without such an analysis Applicant is unable to ascertain with certainty the propriety of the Examiner's rejection including the rationale behind why the skilled artisan would implement such a combination. For example, it is not possible for Applicant to ascertain with any certainty how efficient use of addressing modes would be accomplished. As the rejections of each of claims 1-21 rely upon a similar failure to present a prima facie case of obviousness, the rejections are improper and Applicant request that they be withdrawn.

With particular regard to claims 8-10 and 17-18, Applicant submits that the Examiner's rejection improperly relies upon a recitation of various elements without a proper analysis of how the elements are to be combined. Each of these claims contains a number of specific limitations. The Examiner's rejection makes vague references to returning from an interrupt and the need to restore existing conditions. As stated above, the M.P.E.P. and supporting case law require that the Examiner analyze whether the claimed invention as a whole would have been obvious and that the Examiner should not

improperly attempt to distil an invention down to an alleged 'gist' or 'thrust' of an invention. Thus, the Examiner's rejection is improper because it fails to address the claimed invention as a whole; instead, it appears that the Examiner is attempting to distill various claim limitations down to what the Examiner believes is the "gist" of the invention. For example, it is unclear how the combination of references would correspond to limitations of claim 8 that are directed to register bank block selection data indicative of a pre interrupt switch state. In another example of limitations of claim 8, neither the Examiner nor the references clearly indicated what would correspond to a pre interrupt register bank block selection signal derived from the stored register bank block selection data. As such, it is unclear from the rejection: 1) what aspects of the Fujimura reference correspond to the various claim limitations and 2) how these aspects would function in the asserted circuit of the Mitsuhira reference. Without a showing of correspondence for each claim limitation and an analysis of the limitations as a whole, the rejections cannot stand and Applicant respectfully requests that they be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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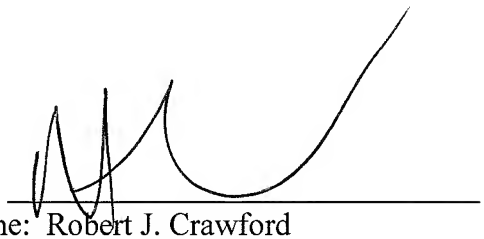
By: 
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